WHAT IS CLAIMED IS:

1. Image processing circuitry, comprising:

a two-dimensional image pipeline that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space;

a three-dimensional image pipeline that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable to perform motion compensation operations associated with said two-dimensional image pipeline in one mode and to perform rasterization operations associated said three-dimensional image pipeline in another mode.

2. The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to sample reference frames in said one mode and to perform texture mapping in said another mode.

3. The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said one mode and to blend samples from a plurality of texture maps in said another mode.

4. The image processing circuitry set forth in Claim 2 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error term in said one mode and to perform alpha blending in said another mode.

5. The image processing circuitry set forth in Claim 1 is operable to support at least one MPEG standard.

6. The image processing circuitry set forth in Claim 1 further comprising an alpha blend sub-circuitry that is operable to process at least 8- and 9-bit signed values.

7. For use in image processing circuitry that comprises a two-dimensional image pipeline and a three-dimensional image pipeline, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating dual mode sub-processing circuitry that is associated with both of said pipelines, said method comprising the steps of:

performing motion compensation operations associated with said two-dimensional image pipeline in one mode; and

performing rasterization operations associated said three-dimensional image pipeline in another mode.

8. The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the steps of:

sampling reference frames in said one mode; and

performing texture mapping in said another mode.

9. The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the step of blending one of samples from a plurality of reference frames in said one mode and samples from a plurality of texture maps in said another mode.

10. The method of operating said dual mode sub-processing circuitry set forth in Claim 8 further comprising the steps of:

processing said plurality of reference frames using error terms in said one mode; and

performing alpha blending in said another mode.

11. The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the step of switching from said another mode to said one mode to perform motion compensation in accordance with at least one MPEG standard.

12. The method of operating said dual mode sub-processing circuitry set forth in Claim 10 wherein said performing alpha blending step further comprising the step of processing at least 8- and 9-bit signed values.

13. The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising the step of controlling said dual mode sub-processing circuitry.

14. Mode control circuitry for use in an image processing system having a two-dimensional image pipeline that processes two dimensional image data to generate successive two-dimensional image frames and a three-dimensional image pipeline that is operable to process three-dimensional image data to render successive three-dimensional image frames, said mode control circuitry comprising:

dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable to perform motion compensation operations associated with said two-dimensional image pipeline and to perform rasterization operations associated said three-dimensional image pipeline; and

a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in one mode and to perform said rasterization operations in said other mode.

15. The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to sample reference frames in said one mode and to perform texture mapping in said other mode.

16. The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said one mode and to blend samples from a plurality of texture maps in said other mode.

17. The mode control circuitry set forth in Claim 15 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error terms in said one mode and to perform alpha blending in said other mode.

18. The mode control circuitry set forth in Claim 14 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

19. The mode control circuitry set forth in Claim 14 further comprising an alpha blend sub-circuitry that is operable to process at least 8-bit and 9-bit signed values.

20. For use in image processing circuitry that comprises a two-dimensional image pipeline and a three-dimensional image pipeline, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating mode control circuitry that is associated with both of said pipelines, said method comprising the step of controlling dual mode sub-processing circuitry to at least one of perform motion compensation operations associated with said two-dimensional image pipeline in one mode, and perform rasterization operations associated said three-dimensional image pipeline in another mode.

21. The method of operating mode control circuitry set forth in Claim 20 further comprising the steps of:

sampling reference frames in said one mode; and

performing texture mapping in said other mode.

22. The method of operating mode control circuitry set forth in Claim 20 further comprising the steps of:

blending samples from a plurality of reference frames in said one mode; and

blending samples from a plurality of texture maps in said other mode.

23. The method of operating mode control circuitry set forth in Claim 21 further comprising the steps of:

processing said plurality of reference frames using error terms in said one mode; and

performing alpha blending in said other mode.

24. The method of operating mode control circuitry set forth in Claim 20 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

25. The method of operating mode control circuitry set forth in Claim 20 further comprising an alpha blend sub-circuitry that is operable to process at least 8-bit and 9-bit signed values.

26. A media processing system having a central processing unit, a memory subsystem, an image processing system, and a display system, said media processing system comprising:

a two-dimensional image pipeline that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of said display system;

a three-dimensional image pipeline that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable to perform motion compensation operations associated with said two-dimensional image pipeline in one mode and to perform rasterization operations associated said three-dimensional image pipeline in another mode.